IN THE CLAIMS:

Claims 1-19 (Cancelled)

20. (Currently Amended) A power semiconductor device comprising:

a substrate having a central region an and outer edge

an active region disposed in the central region of the substrate and defined by first and second regions highly doped with the same or opposite polarity of dopant

an insulating layer over the substrate and between the active region and the edge of the substrate

at least three field plates on the insulating layer and disposed between the active region and the outer edge of the substrate, said field plates each having an outer edge facing the edge of the substrate and an inner edge facing the active region and each having an applied voltage potential such that the voltage potential difference between the first and second field plates is different from the voltage potential difference between the second and third field plates to generate electric fields in the substrate below the field plates wherein said electric fields have substantially the same contours.

21. (Previously presented) The power semiconductor device of claim 20 further comprising means for generating voltage potentials applied to the field plates.

22. (Previously presented) The power semiconductor device of claim 21 wherein the means for generating voltage potentials is a voltage divider network of resistors.

23. (Currently Amended) The power semiconductor device of claim 22 wherein the first and second highly doped regions comprise an emitter and a collector, the voltage divider connected between the emitter and collector and having a plurality of resistors sized to generate the applied voltage for forming the electric fields with substantially similar contours.

24. (Currently Amended) A power semiconductor device comprising:

a substrate having a central region an and outer edge

an active region disposed in the central region of the substrate ~~substrate~~ and defined by first and second regions highly doped with the same or opposite polarity of dopant

an insulating layer over the substrate and between the active region and the edge of the substrate

at least three field plates on the insulating layer and disposed between the active region and the outer edge of the substrate, said field plates each having an outer edge facing the edge of the substrate and in inner edge facing the active region

means for applying different voltage bias levels to each field plate wherein the applied different voltage bias level generates electric fields in the substrate below the field plates and wherein said electric fields below said field plates have contours varying from the outer edge of the each field plate to the inner edge of each field plate and the contours of each electric filed below two or more field plates are substantially the same.

25. (Previously presented) The power semiconductor device of claim 24 wherein the contours of each electric field in the substrates in the regions below each field plate is substantially the same.

26. (Previously presented) The power semiconductor device of claim 24 wherein the means for applying different voltage bias levels comprises a voltage divider network including a plurality of resistive elements connected in series to each other for generating said different bias voltages, each of said bias voltages being dependent at least in part upon a corresponding one of said resistive elements.

27. (Previously presented) The power semiconductor device of claim 26, wherein the first and second highly doped regions comprise an emitter and a collector, said

voltage divider network comprising a serpentine polysilicon resistor electrically connecting said emitter and said collector, said resistor having a length, said field plates being connected to said resistor at respective points along said length thereof.

28. (Previously presented) The power semiconductor device of claim 27, wherein said polysilicon resistor is uniformly doped along its length to provide a continuous resistance between the emitter and the collector.

29. (Previously presented) The power semiconductor device of claim 26, wherein said voltage divider network includes MOSFET devices.

30. (Previously presented) The power semiconductor device of claim 26, wherein said voltage divider network includes a combination of MOSFET devices and resistors.

31. (Previously presented) The power semiconductor device of claim 27 wherein said voltage divider network electrically connects said edge with one of an emitter, source and gate of said power semiconductor device.

32. (Previously presented) The power semiconductor device of claim 27, wherein the bias voltage applied to a particular one of said field plates is dependent at least in part upon the proximity of said particular one of said field plates to said edge.

33. (Previously presented) The power semiconductor device of claim 32, wherein the bias voltage applied to a particular one of said field plates increases with the proximity of said particular one of said field plates to said edge.

34. (Previously presented) The power semiconductor device of claim 32, wherein:

said first field plate is disposed relatively proximate to said edge, said second field plate is disposed between said first and third field plates relative to said edge, and said third field plate is disposed relatively distant from said edge; and

said voltage divider network being connected across a potential difference and generates a first, second and third voltage, said first voltage applied to said first field plate and being from approximately fifty to approximately sixty percent of said potential difference, said second voltage applied to said second field plate and being from approximately twenty to approximately thirty percent of said potential difference, and said third voltage applied to said third field plate and being from approximately fifteen to approximately twenty percent of said potential difference.

35. (Previously presented) The power semiconductor device of claim 34, wherein said first voltage is approximately fifty-seven percent of said potential difference, said second voltage is approximately twenty-five percent of said potential difference, and said third voltage is approximately eighteen percent of said potential difference.

36. (Previously presented) The power semiconductor device of claim 27, wherein said voltage divider network is integral and monolithic with said die.

37 (Previously presented) The power semiconductor device of claim 27, wherein each of said plurality of field plates has a predetermined and respective width, said widths of said field plates being separately adjusted dependent at least in part upon a voltage rating of said power semiconductor device.

38. (Previously presented) The power semiconductor device of claim 27, wherein each of said field plates is separated from adjacent field plate(s) by a predetermined and respective distance, said distances being adjusted dependent at least in part upon a voltage rating of said power semiconductor device.

39. (Currently Amended) A method of controlling the electric field concentration on the outside edge of a power semiconductor device comprising

in a substrate having a central region and an edge, forming an active region of a power semiconductor device comprising first and second regions highly doped with dopants of the same or opposite polarity

forming an insulating layer between the active region and the edge

disposing a plurality of field plates on said die, said field plates being spaced apart relative to each other;

dividing a potential difference to generate a different bias voltage for each field plate

applying the respective different potentials to the respective field plates to generate electric fields in the substrate that have substantially the same electric field contours.

40. (Previously presented) The method of claim 39, wherein said dividing step comprises electrically connecting one or more polysilicon resistors between said edge and one of an emitter and gate of said power semiconductor device.

41. (Previously presented) The method of claim 39, wherein said dividing step comprises electrically connecting a series combination of resistors between said edge and one of an emitter and gate of said integrated circuit.

42. (Previously presented) The method of claim 39, wherein said dividing step comprises electrically connecting a combination of resistors and MOSFET devices between said die street and one of an emitter and gate of said integrated circuit.

43. (Previously presented) The method of claim 39, wherein:

said disposing step comprises disposing first, second and third field plates on said die, said first field plate being relatively proximate to said die edge, said second field plate being disposed between said first and second field plates, and said third field plate being disposed relatively distant from said die street and proximate the active region; and

said applying step comprises applying a first, second and third bias voltage to said first second and third field plates, respectively, said first bias voltage having a value of from approximately fifty to approximately sixty percent of said potential difference, said second bias voltage having a value of from approximately twenty to approximately thirty percent of said potential difference, and said third bias voltage having a value of from approximately fifteen to approximately twenty percent of said potential difference.

44. (Previously presented) The method of claim 43 wherein said first bias voltage is approximately fifty-seven percent of said potential difference, said second bias voltage is approximately twenty-five percent of said potential difference, and said third bias voltage is approximately eighteen percent of said potential difference.